International Journal of Advanced Computer and Mathematical Sciences.
Vol 1, Issue 1, Dec, 2010, pp 12-16. http://bipublication.com

METHOD TO MINIMIZE THE CLOCK SKEW IN MULTIPLE PIPE LINE BY UNIFORM CLOCK DISTRIBUTION USING PARALLEL PORT

[1] N. Suresh Kumar, [2]D.V. RamaKotiReddy, [3]S.Praveen, [4]J.Anitha, [5]G.Brahmaji

[1, 3, 4] Dept of IT, GITAM University, Visakhapatnam
[2] College of Engineering, Andhra University, Visakhapatnam
[5] Nobel Institute of Science and Technology, Visakhapatnam

ABSTRACT

This paper presents a new pipeline method with jitter removal technique. The conventional pipeline system is facing problems due to improper synchronization of clock pulses. This is a universal problem in all the digital systems mostly called jitter or skew. Here a new system is implemented in the path of the clock to remove or reduce the clock skew. The jitter is also introduced in the pipeline due to different clock paths to the parallel pipelines. While one pipeline access the data pulses the remaining pipelines remain in idle state as single clock pulse is used to fed encoder pulses. And it creates a big challenge if multiple clock pulses are given to individual pipeline systems. This can be overcome using parallel ports as clock signals. The hardware configuration and algorithms for a microcontroller implementation are also presented.

Keywords: Parallel Pipeline, Clock Skew, Parallel port, Microcontroller, Synchronization, High Performance.

I INTRODUCTION

In most of the digital systems a two stage pipeline [4] is used for faster data rates. And it is also limited for some extension only. The conventional pipeline system is facing problems due to improper synchronization of clock pulses. This is a universal problem in all the digital systems mostly called jitter or skew.

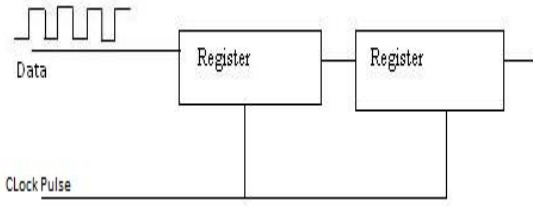

Figure 1 Conventional pipeline System

In conventional pipeline systems the clock signal is derived as [1]

$$T_{clk\_conv} \geq D_{max} + D_r + T_s + \Delta_{clk}$$

Here a new system is implemented in the path of the clock to remove or reduce the clock skew. The jitter is also introduced in the pipeline due to different clock paths to the parallel pipelines. This can be reduced using by controlling the clock pulses supplied to the parallel pipelines. There may be a chance of problem in applying clock pulses to parallel pipelines simultaneously. This can be avoided by supplying clock pulses

using parallel ports available at microcontroller instead of using external timer or counter. But in the case of microprocessor which does not have internal port architecture an external port device need to interface to supply pulses to the pipelines simultaneously.

II PIPELINE OPERATION

Pipeline is a technique used to design high-performance digital systems. In the pipeline series multiple stages are integrated to reduce the data loss when compared to conventional systems. In a pipelined system, pipeline stages operate on different data vectors/waves simultaneously and each stage on only one data wave at any given time [1]. In the present work a two stage pipeline is integrated in the design. The system has cascaded SISO shift registers with the common clock pulse supplied by decoder output, to retain the next data and push the current data to the next stage. As the data enters into the next stage, the vacated bit position in SISO Shift register is filled with the next bit. And a new bit will be inserted into the first bit of pipeline. This will improve the data transmission rate and reduces the data loss in wait states and not ready sequences.

A two stage pipeline system is integrated in the circuit to achieve best hit ratio. Here the individual bits of the data are fed to registers and they are pushed serially. The bits are temporarily stored in the registers.

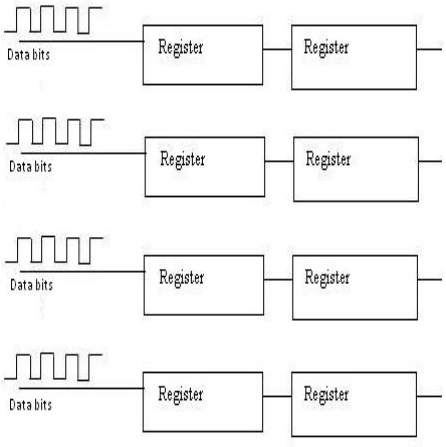

Figure 2 multiple pipeline System

Equation (1) defines the clock period for a pipeline system; Where D_{max} is the largest of maximum propagation delay of all stages in the pipeline [4][1].

$$T_{clk} \geq D_{max} + D_R + t_s + \Delta clk \quad \text{----------} \quad (1)$$

For (1) to be valid, the following condition must be satisfied.

$$D_{min} + D_R \geq t_h + \Delta clk \quad \text{----------} \quad (2)$$

The condition in (2) ensures that new data does not appear at input of a register before its hold time is up.

T_{clk} = clock period

Δ = Constructive clock skew

Δclk = Clock uncertainties

t_h = Pipe line register and hold time

t_s = Pipe line registers setup time

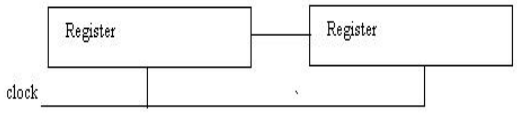

Figure 3 clock connected to two registers

A single clock pulse is applied to manage the data transmission through

the registers in the pipeline. But it will create a clock skew in the pipeline which will decrease the data speed from one stage to other stage. The data bits are fed into the first register only when clock pulse is applied to the first stage of the pipeline. The pulse will be passed to the next stage after applying the clock pulse to the next stage. The clock pulse path is directly given to the registers where the data bits are passes from one stage to another stage through flip flops of the registers. This may create a problem of overlapping of pulses in the first stage before it enters into the next stage.

So to avoid this overlapping a delay element is included in the path of the clock pulse. This delay will be equal to the delay created by the pulse passed from one stage to other stage [4].

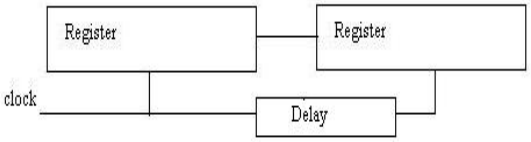

Figure 4 A delay inserted in clock path to remove clock skew

The clock signal is derived in the Mesynchronous pipelining is [4]

$$T_{clk\_m} \geq \left(D_{max\,(j)} - D_{min\,(j)}\right) + t_h + T_s + 2\Delta_{clk}$$

Where D_{min} is the minimum propagation delay of all stages in the pipeline [4][1].

The present system also performs with the same timing signals as shown in the above equation. But a parallel pipeline is effectively operated in the present system than the other methods.

At the same it is required to consider the clock pulses applied to the individual stages in parallel pipeline system. It is very difficult to control all the clock pulses for all the four pipelines.

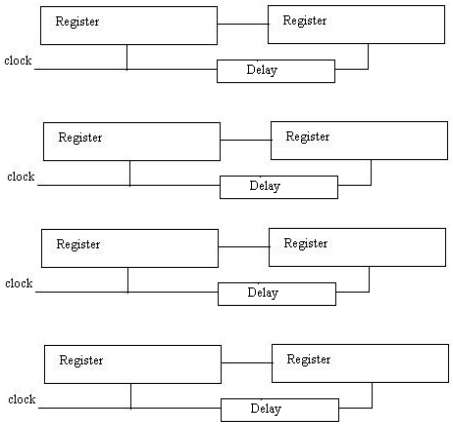

Figure 5 Parallel pipeline system

Equation (1) defines the clock period for a pipeline system; Where D_{max} is the largest of maximum propagation delay and D_{min} is the minimum propagation delay of all stages in the pipeline [4].

$T_{clk} \geq D_{max} - D_{min} + D_R + t_s + \Delta clk$ ---------- (3)

So,

$D_{max} - D_{min} < T_{clk} - (D_R + t_s + \Delta clk)$---------- (4)

So here a method is developed to distribute the clock pulses evenly to get the same performance as shown in equation (4). All the clock pulses are simultaneously supplied through programmable parallel port. These parallel ports are independently control the clock supply to the individual pipelines. These ports are programmed by defining control word in the microcontroller. The ports are defined as output ports to supply the clock

pulses to the pipelines. The width of the clock pulse is decided by the internal software delay branched in between high to low state on the port pin.

III HARDWARE CONFIGURATION

But while enabling one pipeline system the remaining pipeline systems remain in idle state in figure 4. This wastage of time can be reducing by interfacing clock system with parallel ports. A parallel port is used to select the pipeline in sequence and it also used to produce necessary clock pulses for pipelines. When the microprocessor enables the first output port pin, then the first pipeline carries the data bits or data pulses to the next stages. The port outputs are enabled simultaneously to enable other pipelines in the same time. So here four port pins are used to supply the clock pulses. And no external or internal timer and counter are used for clock pulses.

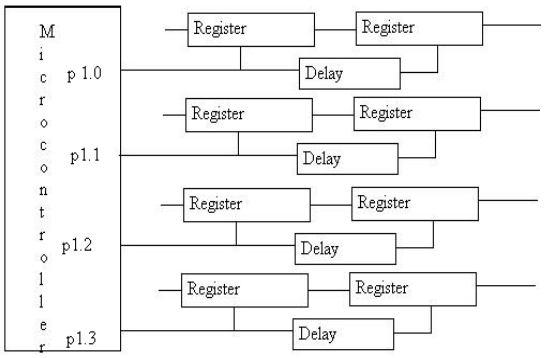

Figure 6 Parallel port clock system for parallel pipelining system

The clock signal is derived in the present system pipeline method as,

$$T_{mc\_clk\_p} > \left(D_{max(ij)} - D_{min(ij)}\right) + t_h + T_s + 2\Delta_{clk}$$

So the timing signals can be comparing in wave pipelining, conventional and present system as

$$T_{mc\_clk\_p} \leq T_{clk\_w} \leq T_{clk\_conv}$$

From this the system performance somewhat similar to Mesynchronous pipelining.

IV SOFTWARE ROUTINES

Step 1: Define four port pins as output ports.

Step 2: Send a high and low signals alternatively through parallel port to enable clock input to the pipelines.

Step 3: Repeat from step3 to step 5 as per the user requirement to take the average values.

The code is developed in assembly level language using MASM software. The pipeline operations are observed in CAD software.

V CONCLUSIONS

The main problem clock skew in conventional method are reduced using pipelines and can also by introducing delay paths in the clock path to the pipelines. In parallel pipelining while enabling one pipeline using single clock system the remaining pipeline systems remain in idle state. The jitters due to multiple pipelines are minimized by applying clock pulses through parallel ports simultaneously. The cost effect is less when compared to other methods performances. It avoids the time constraints in accessing data bits. Further the execution time can be improved using

ARM processor. In pipeline technology a multiple clock pulses are applied to the pipeline stage through a decoder and so there is no timer and counter circuit needed to control the clock pulses at different register levels. This delay path in the clock pulse to the pipeline improves the data transmission rate and reduces the data loses in wait states and not ready sequences and reduces the clock skew. At a time multiple numbers of pipelines can be accessed using parallel port clock system.

REFERENCES

1. C. Thomas gay, "Timing constraints for wave pipelined systems" IEEE transactions on Computer aided design of integrated circuits, vol13, no.8, august 1994.
2. Jabulani Nyathi, "A high performance hybrid wave pipelined linear feedback shift register with skew tolerant clocks", IEEE, 1384-1387, 2004.
3. Mohammad Maymandi, "A digital programmable delay element: Design and analysis", IEEE transaction VLSI systems, Vol.11, no.5, October 2003.
4. .Suryanarayana B. Tatapudi, *Student Member, IEEE* and José G. Delgado-Frias, *Senior Member, IEEE,*A Mesychronous high performance digital systems, VOL. 53, NO. 5, MAY 2006.
5. Wayne P. Burleson, "Wave-Pipelining: A Tutorial and Research Survey", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 6, NO. 3, SEPTEMBER 1998